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Research on Parameter Optimization of SMT Based on Intelligent Image Recognition and Taguchi Engineering Technology

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ABSTRACT

This study focuses on the Surface Mount Technology (SMT) during the reflow soldering stage. It utilizes the Taguchi Engineering optimization parameter design to enhance the soldering process and employs artificial intelligence image recognition to detect and calculate the void diameter. The study uses a L_{18} orthogonal array for the experiments and aims to identify the optimal combination of factor levels that reduce the occurrence of void by improving the stencil, squeegee, and pad aperture. The results of the study show that the proposed parameter levels can effectively minimize the occurrence of void, enhance the yield process, and ensure product quality.

Keywords: image recognition algorithm, Taguchi engineering, surface mount technology

結合人工智慧影像辨識與田口工程技術於 SMT 最佳化參數設計之研究

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摘　　要

表面黏著技術(Surface Mount Technology, SMT)是指將電子元件安裝在印刷電路板(PCB)表面的方法。而錫洞(Void)為 SMT 製程中常見的不良現象之一，其容易導致產品功能的失效，因此為製程品質檢核的重點項目。其流程可分為四個主要步驟：焊膏印刷、元件貼裝、回流焊接和最終檢查。本研究主要探討表面黏著技術於回焊階段，以田口工程最佳化參數設計針對缺陷之影響因子進行改善，並透過人工智慧影像辨識來檢測並計算錫洞/焊點直徑總合佔比。以印刷鋼板、刮刀和載板開槽的參數為控制因子，並以 L_{18} 直交表進行實驗設計，試圖找出製程的最佳參數水準組合。實驗證明新的參數水準組合有效降低了錫洞現象的發生，進而提升了製程的良率，確保產品的品質。

關鍵詞：影像辨識演算法，田口工程，表面黏著技術

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I. INTRODUCTION

Over the years, electronic products have become lighter, thinner, shorter, smaller, and more powerful. To keep up with the market demands and trends, electronic components have had to be reduced in size, leading to the development of Surface Mount Technology (SMT), which can be directly adhered to the Printed Circuit Board (PCB). Furthermore, PCBs have evolved from single-layer to multi-layer boards to reduce their size, leaving no extra space for traditional components and through-holes.

The SMT technology was created to attach SMD (Surface Mount Device) components onto a PCB. However, due to advancements in SMT technology, the requirements for the solder paste printing process are increasing. Component pin distances are getting smaller, component density is increasing, and pin designs are becoming more complex, making it difficult to control the process. Therefore, controlling the solder paste process is crucial in improving the yield of SMT.

This study is dedicated using the Taguchi engineering optimization parameter design method to explore the impact factors that cause soldering defects in the reflow soldering stage of SMT, proposes improvement methods to improve them, and also researches and designs a set of artificial intelligence image recognition process to accelerate and replace the time-consuming and inaccurate manual inspection.

II. LITERATURE REVIEW

Based on the market needs and trends mentioned above, products have increased functional density and reduced input/output spacing. Electronics manufacturers will also face the problem of cutting down solder defects and improving solder paste inspection technology. They are committed to developing robust SMT processes to enhance the stability of a process and even try to find the optimal combination of parameters for SMT processes. Many studies have pointed out that the critical process of SMT is solder paste printing; about 50%-70% of solder joint defects are related to this process [1-4].

Therefore, more and more researchers have begun trying to improve the solder paste printing process, using various technologies to improve process capabilities to reduce product variation and improve product quality. They use the Six Sigma-DMAIC (Define, Measure, Analyze, Improve, Control) improvement processes to optimize the process parameters that improve the quality of SMT solder paste printing processes [5-8].

Chang et al. investigated a defect recognition model for the solder paste printing process of SMT products based on multi-source and multi-dimensional data reconstruction [9]. The model correlates features and defects, which improves quality control processes through feature interaction, selection, and conversion. Acciani et al. developed an automatic inspection system using neural networks to detect solder joint defects on printed circuit boards [10]. The system compares three classifiers with three types of feature vectors and five types of solder joints to evaluate the region of interest.

Taguchi method prioritizes the effective implementation of engineering strategies over advanced statistical techniques to achieve cost-driven quality engineering. Chang utilized the Taguchi method to explore the dependency between deposited solder paste volume in the five key process parameters to minimize product variation in SMT solder paste processes [2]. Tu used the DMAIC approach to identify the critical factor and then applied the Taguchi method to achieve the ultimate process parameters in SMT solder paste printing [8]. Jou et al. utilized TRIZ methodology to identify the four most influential parameters on SMT solder paste thickness: squeegee pressure, ejection speed, squeegee speed, and squeegee angle. Then, the Taguchi method determines the best combination of parameter levels [11].

Lin and Kuo studied the feasibility of using Taguchi accumulative analysis method to improve SMT process parameters [12]. Fig. 1 shows the solder paste printing architecture. The study mainly uses adjusting the parameter levels of control factors such as the physical specifications and operation behaviors of Stencil and Squeegee as the research method and doesn't add innovative improvement methods. However, the height of the pressing and pad aperture are the critical improvement factors not investigated. Thus, this study attempts to reduce the occurrence rate of voids by adding control factors such as pad aperture shown in Fig.2. and height of pressing to avoid product failure.

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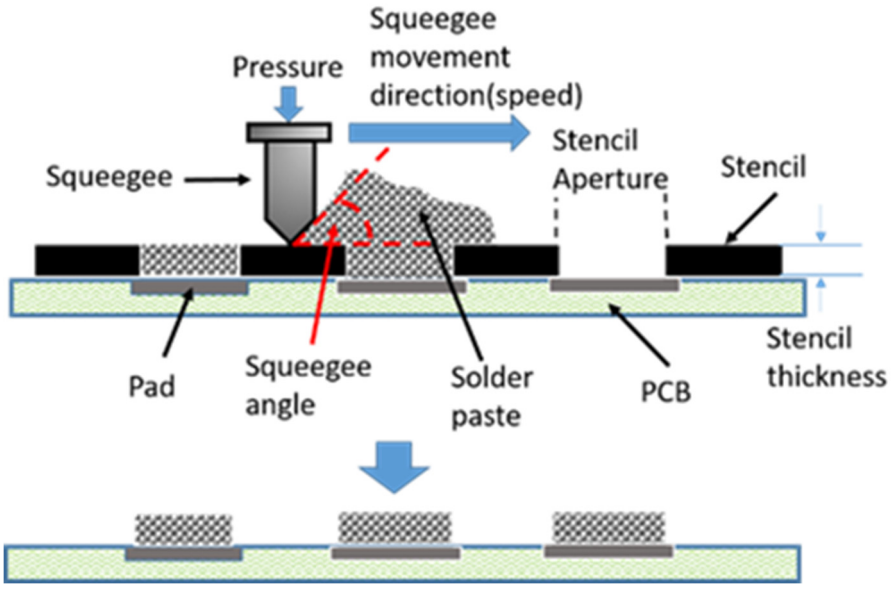

Fig.1. Solder paste printing architecture

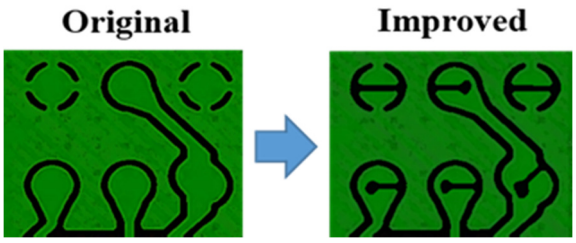

Fig. 2. Pad aperture diagram

III. METHODOLOGY

3.1 The SMT processes

SMT is a method that attaches electronic components onto the surface of PCB. It solders SMD onto the boards through reflow soldering. The process of SMT manufacturing is shown in Fig. 3. And the process steps are described as follows:

1. Material preparation and examination
   Prepare PCBs and SMDs and check for defects. PCBs typically have flat, usually tin-lead, silver-plated, or gold-plated, non-porous copper pads.
2. Stencil preparation
   Usually, we use the stencil to provide a fixed position for solder paste printing; it depends on the pad position designed on the PCB to produce.
3. Solder paste printing
   Solder paste is usually a mixture of flux and tin; we use solder paste to connect the SMDs and pads onto the PCB. It is applied to PCB with stencil on a angle range of 45°-60° using a squeegee.
4. SMD placement
   A conveyor belt transports the printed PCB to a pick-and-place machine where electronic components are mounted onto it.

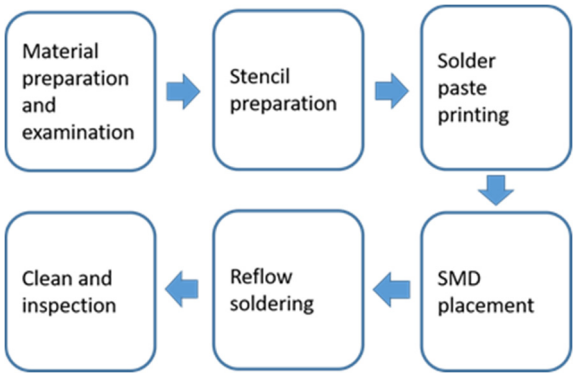

Fig.3. Flow chart of SMT manufacturing process

5. Reflow soldering
   Once the SMDs have been placed on the pads, the circuit board is moved onto a reflow oven for solder paste resoldering, where it undergoes pre-heating, soaking, reflow, and cooling.
6. Clean and inspection
   The PCB undergoes a cleaning process after soldering and inspection for any defects. Inspection methods include visual inspection using a magnifying glass,

automatic optical inspection (AOI), flying probe testing, X-ray machine testing, and more.

3.2 Identification of quality characteristics, control factors and their levels

This study investigates the ratio of the sum of void diameter to the overall diameter as the key quality characteristic. The eight control factors are determined using engineering knowledge. The quality characteristic, void diameter, is affected by eight factors. Two of these factors have two levels, whereas the other six factors have three levels. The eight factors are as follows: Factor A is the height of pressing, which is the height of the squeegee pressing down to the stencil. Factor B is the number of printings, which is the time of solder paste printing onto the pad. Factor C is the snap-off, which is the distance from the PCB's top surface to the stencil's bottom surface. Factor D is the stencil aperture, which is the size of the stencil aperture. Factor E is the squeegee speed, which is the velocity of the squeegee traversing across the stencil. Factor F is the Pad aperture, which opens an exhaust slot on the pad. Factor G is the squeegee pressure, which is the total force of the squeegee pushing onto the pad. Factor H is the angle of attack, which is the angle of the squeegee blade about the stencil. Table 1 shows the eight control factors and their levels.

Table 1. Control factors and their levels (the underline level is the existing level)

Factors	Levels		
	1	2	3
A. Height of pressing	0.2mm	0.3mm	
B. Number of printings	5 times	10 times	15 times
C. Stencil thickness	0.11mm	0.12mm	0.13mm
D. Stencil aperture	90%	100%	110%
E. Squeegee Speed	70-75mm/sec	65-70mm/sec	60-65mm/sec
F. Pad aperture	none	slotted	
G. Squeegee Pressure	5kg/cm^2	6 kg/cm^2	7 kg/cm^2
H. Squeegee Angle	45°	50°	55°

Table 2. Summary of experimental data

Factors and their levels in L_{18}									Experimental result					
Factor Column	A	F	B	C	D	E	G	H	Void Diameter (%)					
No.	1	2	3	4	5	6	7	8	Observation				Average	η
1	1	1	1	1	1	1	1	1	21	22	20	21	21	-26.45
2	1	1	2	2	2	2	2	2	25	26	27	25	25.75	-28.22
3	1	1	3	3	3	3	3	3	43	44	45	43	43.75	-32.82
4	1	2	1	1	2	2	3	3	15	14	14	16	14.75	-23.39
5	1	2	2	2	3	3	1	1	23	24	24	25	24	-27.61
6	1	2	3	3	1	1	2	2	20	21	22	20	20.75	-26.35
7	1	3(2)	1	2	1	3	2	3	16	17	16	15	16	-24.09
8	1	3(2)	2	3	2	1	3	1	34	35	34	33	34	-30.63
9	1	3(2)	3	1	3	2	1	2	19	20	19	18	19	-25.58
10	2	1	1	3	3	2	2	1	37	36	38	37	37	-31.37
11	2	1	2	1	1	3	3	2	20	21	20	21	20.5	-26.24
12	2	1	3	2	2	1	1	3	27	26	25	27	35	-28.39
13	2	2	1	2	3	1	3	2	25	24	23	24	24	-27.61
14	2	2	2	3	1	2	1	3	25	24	26	25	25	-27.96
15	2	2	3	1	2	3	2	1	16	17	16	16	16.25	-24.22
16	2	3(2)	1	3	2	3	1	2	35	36	35	35	35.25	-30.94
17	2	3(2)	2	1	3	1	2	3	18	18	16	17	17.25	-24.75
18	2	3(2)	3	2	1	2	3	1	20	19	21	20	20	-26.03

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3.3 Orthogonal array and factor assignment

To conduct a matrix experiment with two factors having two levels and six factors having three levels, a minimum degree of freedom of 14 is required. It means that an appropriate orthogonal array is L_{18}. Factor A has two levels; we assign it to the first column. All Factors B, C, D, E, G, and H have three levels; we allot them to columns 3 through 8, respectively. Also, we assign Factor F to the 2nd column with the dummy-level technique. While the existing level F1 is required to obtain more precise information for F2, the number of experiments for F2 is increased from 6 to 12. Table 2 lists Factor F and its alternate levels.

3.4 AI Image recognition technology for void detection

This paper proposes a methods to detect circuit board defects using image processing and AI-powered image recognition. The experimental environment is described as follows: (1) Hardware specifications: CPU: Intel Xeon Silver 4214 2.20 GHz, GPU: NVIDIA GeForce GTX 1080 Ti, RAM: 32GB. (2) Software version: Windows version: windows 10, IDE version: PyCharm Community Edition 2020.2.3, Python version: 3.6, Numpy version: 1.19.2, OpenCV version: 4.4.0.46, Tensorflow gpu estimator version: 2.4.0. The proposed method is described in the following steps. Fig. 4. illustrates the system architecture and the resulting outputs.

1. Instant shooting

   For obtaining high-quality X-ray images, it is essential to have stable shooting conditions; this includes sufficient light, the right angle and direction, good contrast, sufficient resolution, appropriate focal length, and a stable shooting mechanism. Additionally, image pre-processing is also crucial.

2. Image pre-processing

   Due to the complexity of PCBs and their color changes, direct image recognition can result in a high rate of identification errors. Therefore, image pre-processing is necessary to reduce unnecessary features in the image and strengthen the features that need to be recognized. We implement the following three image processing processes to fulfill the requirements of subsequent AI image recognition.

   (1) Color to Gray: It is a method of converting color images into grayscale images, which is actually a weighted average of the pixel values of R, G, and B channels, and Eq. 1 shows the calculation expression.

   $$G = 0.299 * R + 0.587 * G + 0.114 * B \quad (1)$$

   (2) Median Filter: Its advantage lies in its ability to effectively deal with different types of noise, such as salt-and-pepper noise in X-ray images. Noises are removed and smoothed. Eq. 2 shows the formula.

   $$B(x,y) = median\{I(x+i, y+i): i = -a, -a+1, ..., a; j = -b, -b+1, ..., b\} \quad (2)$$

   $B(x,y)$ is the pixel value filtered by the median value $\{I(x+i, y+i)$ is the pixel value in the window, and i and j are the horizontal and vertical offsets of the window, respectively.

   (3) Threshold: Convert a grayscale image to an image with only two values, usually 0 and 255, i.e., black and white. The purpose of this process is to emphasize or retain important information in the image while discarding unnecessary details, as described in Eq. 3.

   $$B(x,y) = \begin{cases} 0, & if\ I(x,y) < T \\ 255, & if\ I(x,y \geq T \end{cases} \quad (3)$$

3. Defects detection with an AI image recognition defects

   AI image recognition uses artificial intelligence (AI) technology to train a computer system to recognize and understand images, which can easily enable computers to find the type, size, and location of objects in images. It usually includes the following steps and techniques: (1) Collection and annotation of training data. (2) Preprocessing of training data. (3) Choose the correct model architecture. (4) Model training. (5) Validation and testing. (6) Optimization. (7) Deployment.

This research implements an AI image recognition with the open-source YOLO v7[13]. We perform the solder joint positioning and solder defects detection in two steps: (1) Find solder joints: We have an AI image recognition on the circuit board diagram with pre-processing image and find the size and position of the solder joints in the diagram. Then, we cut the solder joint images and recorded sequentially. (2) Soldering defect detection: Based on all solder joint images found by Find Solder joints, AI image recognition is performed on each solder joint image to find whether there is a defect and output the location and size of the defect.

4. Image post processing

   Through the image post-processing technology, the solder joint defects identified by the AI image are coated with translucent red dots of the same size as the defects at the same position in the original image, visually highlighting the solder joint defects and enabling quality inspectors to find the defects quickly.

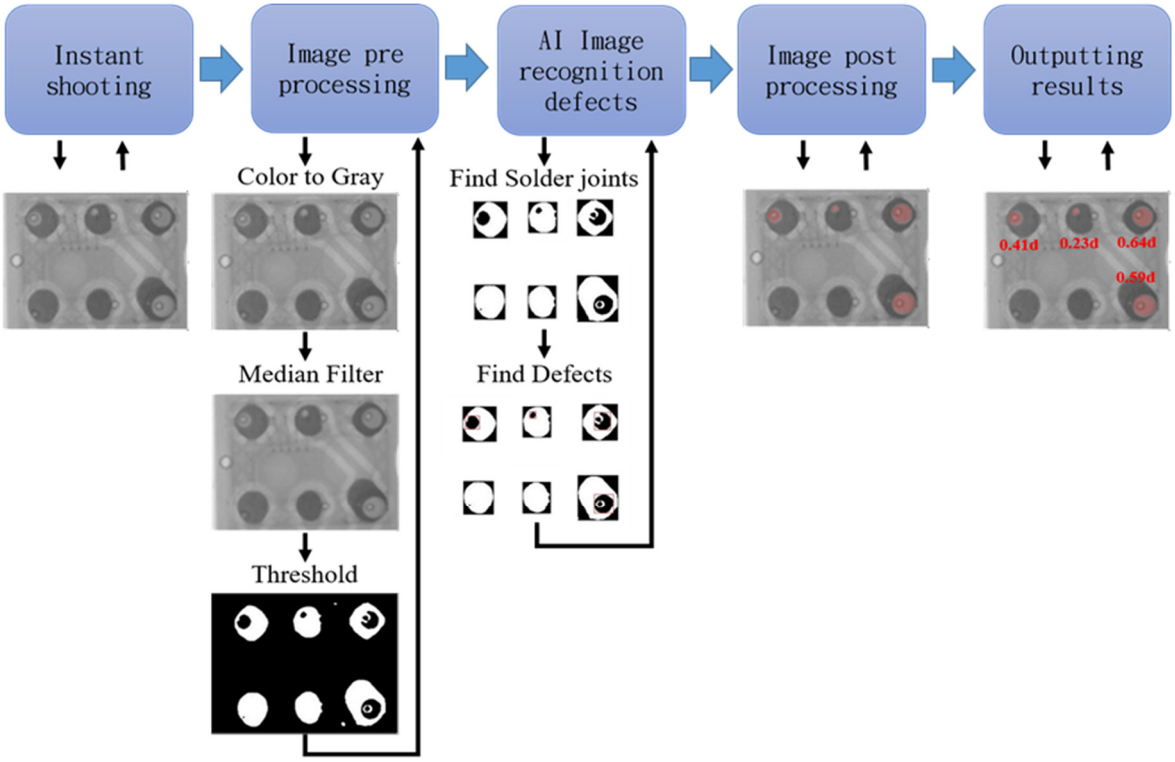

Fig.4. AI image recognition steps and the system architecture and results.

5. Output results

   We calculate the d value of each solder joint defect, and the closer the d value is to 1, the worse the welding quality is, and the better the soldering quality is not. Eq. 4 shows the d-value calculation expression, and the system will mark the d-value of defective solder joints in real-time.

$$d = \frac{Defects}{Solder\ joints} \tag{4}$$

According to IPC7095 7.4.1.6, the general electronics industry requires a total pore diameter of < 30% for Class III. If the void is too large, it will cause air soldering or solder breakage. Fig. 5. shows the schematic.

IV. IMPLEMENTATION OF THE EXPERIMENT AND DATA ANALYSIS

This section introduces the implementation steps of this study and the definitions of related technologies as follows.

4.1 Data analysis

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1. Computation of signal-to-noise ratio
   In accordance with Taguchi [14] and Phadke [15], the signal-to-noise ratio(η) for STB-type quality characteristics can be computed as shown in Eq. 5.

$$\eta = -10log_{10}(MSD) = -10log_{10}\left(\frac{1}{n}\sum_{i=1}^{n} y_i^2\right) \quad (5)$$

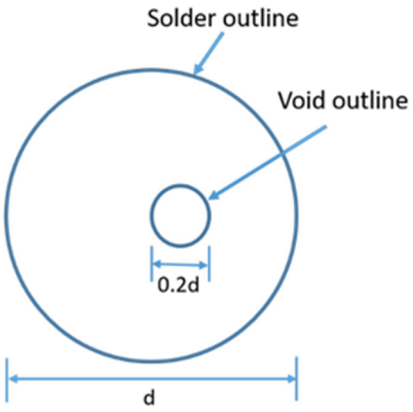

Fig.5. Void size diameter schematic

   where MSD is the mean square deviation, y_i is the quality characteristic and n is the number of replications in each trial.

2. Analyze of variance for the signal-to-noise ratio
   The average signal-to-noise ratio, $\bar{\eta}$, Table 3 shows for each factor level and ANOVA of for void diameter. The degree of freedom for error is 3. The smallest four signal-to-noise ratios are the error terms. That is, the sum of the squares due to Factor A, B, E, and H are not significant. Therefore, the degree of freedom after pooling the error terms is 7.15.

3. Confidence interval for each factor
   Ross defined the confidence interval for the average signal-to-noise ratio, $\bar{\eta}$ [16], for each factor level as shown in Eq. 6.

$$\bar{\eta} \pm \sqrt{F_{(\alpha;\nu_1,\nu_2)} \times V_e \times \left(\frac{1}{n}\right)} \quad (6)$$

   where α represents the significance level and ν1 represents the degree of freedom for the mean. The estimation for ν1 will always be 1 for the confidence interval. ν_2 is the degree of freedom for the pooled error term, V_e is the pooled error variance equivalent to Eq. 7. and n is the number of replications in each trial.

$$V_e = \frac{sum\ of\ squres\ due\ to\ error}{degrees\ of\ freedom\ for\ error} \quad (7)$$

For void diameter, $V_e = \frac{7.15}{10} = 0.72$. Let α =5%, then 95% confidence interval of $\bar{\eta}$ for each level is computed as follow:

$$\bar{\eta} \pm \sqrt{F_{(0.05;1,10)} \times 0.72 \times \left(\frac{1}{4}\right)} = -25.1 \pm 0.95$$

4.2 Combinations of the optimum parameter level

Based on the ANOVA analysis of void diameter in Table 3, it determines that Factors C, F, D, and G are significant among the eight control factors, while the remaining factors remain at their original levels. Among C_1, D_1, F_2, and G_2, the signal-to-noise ratio is higher. This means that the optimal parameter level for the void diameter is $A_1B_2C_1D_1E_2F_2G_2H_1$.

4.3 Prediction of signal-to-noise ratio

The sum of the squares of the void diameters caused by Factors A, B, E, and H is negligible. Since these terms are considered errors, we do not consider the corresponding improvement in the η prediction under optimal conditions. If we include the contribution of all factors, the predicted improvement in n exceeds the actual achieved improvement. That said, forecasts will be on the high side. Ignoring factors that contribute less to the sum of mean squares, the error will be reduced.

The existing parameter level combination is $A_1B_2C_2D_2E_2F_1G_1H_1$, and the corresponding signal-to-noise ratio, for the void diameter is computed as follows:

$$\eta_{old} = \bar{\eta}A_1 + \bar{\eta}B_2 + \bar{\eta}C_2 + \bar{\eta}D_2 + \bar{\eta}E_2 + \bar{\eta}F_1 + \bar{\eta}G_1 + \bar{\eta}H_1 - 5\bar{\eta} = -28.47\ (\text{bB})$$

The optimum parameter level for the void diameter is $A_1B_2C_1D_1E_2F_2G_2H_1$. The predicted signal-to-noise ratio, η_{opt}, for the void diameter is computed as follows:

$$\eta_{opt} = \bar{\eta}A_1 + \bar{\eta}B_2 + \bar{\eta}C_1 + \bar{\eta}D_1 + \bar{\eta}E_2 + \bar{\eta}F_2 + G_2 + \bar{\eta}H_1 - 5\bar{\eta} = -22.28\ (\text{dB})$$

The improvement for the void diameter is

$\Delta\eta = \eta_{opt} - \eta_{old} = -22.28 - (-28.47) = 6.19(\text{dB})$. Thus, the void diameter in the optimum parameter level combination is 0.62 times that of the existing parameter level combination, as shown in the following:

$$\left(\frac{y_{opt}}{y_{old}}\right)^2 = 10^{\frac{-\Delta\eta}{10}} = 10^{\frac{-6.19}{10}} = 0.38$$

$$y_{opt} = 0.62 \text{ x } y_{old}$$

A confidence interval for the optimum parameter level combination, η_{opt}, is shown in Eq. 8:

$$\eta_{opt} \pm \sqrt{F_{(\alpha;\nu_1,\nu_2)} \times V_e \times \left(\frac{1}{n_{eff}}\right)} \quad (8)$$

where n_{eff} is the effective sample size equivalent to Eq. 9.

$$n_{eff} = \frac{Total\ number\ of\ experiment}{1+\left[\begin{matrix}total\ degrees\ of\ freedom\ associated \\ with\ items\ used\ in\ \eta_{opt}\ estimate\end{matrix}\right]} \quad (9)$$

The value of n_{eff} for void diameter is $\frac{18}{1+7}$. Therefore, 95% confidence interval of is computed as follows:

$$\eta_{opt} \pm \sqrt{F_{(0.05;1,10)} \times 0.72 \times \left(\frac{8}{18}\right)} = -22.28 \pm 1.26$$

4.4 Confirmation experiment

Table 4 shows the confirmation experiment under the combination of the optimum parameter level with four replicates for verification. The confidence interval for the signal-to-noise ratio, $\eta_{confirm}$, for the verification experiment is shown in Eq. 10.

Table 3. ANOVA of η for void diameter

Factor	Average η for factor level (dB)			Degree of	Sum of	Mean	F	Contribution
	1	2	3	freedom	squares	square	value	percentage(P%)
A. Height of pressing	-27.24	-27.50	-	1	0.31	-	-	-
B. Number of printings	-27.31	-27.57	-27.23	2	0.37	-	-	-
C. Stencil thickness	-25.10	-26.99	-25.72	2	73.56	36.78	51.42	58.69
D. Stencil aperture	-26.19	-27.63	-28.29	2	13.89	6.94	9.71	10.14
E. Squeegee Speed	-27.36	-27.09	-27.65	2	0.95	-	-	-
F. Pad aperture	-28.13	-26.60	-	1	21.48	21.48	30.03	16.89
G. Squeegee Pressure	-27.82	-26.50	-27.79	2	6.82	3.41	4.77	4.39
H. Squeegee Angle	-27.72	-27.49	-26.90	2	2.14	-	-	-
Error				3	3.38	-	-	-
(The pooled error)				10	7.15	0.72		9.89
Total				17	122.90	7.23		100

Table 4. Verification experiment data

Experiment condition (matrix experiment)								Experimental result Void Diameter (%)					
A	F	B	C	D	E	G	H	Observation				Average	η
1	2	2	1	1	2	2	1	14	15	13	15	14.25	-23.09

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$$\eta_{opt} \pm \sqrt{F_{(\alpha;\nu_1,\nu_2)} \times V_e \times (\frac{1}{n_{eff}} + \frac{1}{r})} \quad (10)$$

where r is the number of replicates of the verification experiment. Therefore, the 95% confidence interval, $\eta_{confirm}$, for the void diameter is computed as follows:

$$-22.28 \pm \sqrt{F_{(0.05;1,10)} \times 0.72 \times \left(\frac{8}{18} + \frac{1}{4}\right)}$$

$$= -22.28 \pm 1.57$$

V. CONCLUSIONS

SMT is a new technology in PCB manufacturing, and the reflow soldering step is one of the critical processes of SMT. In this study, we can improve the occurrence of soldering defects(voids) effectively through the process improvement of pad aperture shown in Fig. 6., and we can enhance the detection accuracy through artificial intelligence image recognition technology. The results show that: (1) The quality characteristic, void defect, was determined by engineering knowledge. The control factor tried in this study, pad aperture, effectively improved solder joint defects. (2) The optimal combination of parameter levels was determined using the Taguchi method with a L_{18} matrix experiment. (3) Artificial intelligence image recognition technology improves the speed and accuracy of manual interpretation of defects in the process.

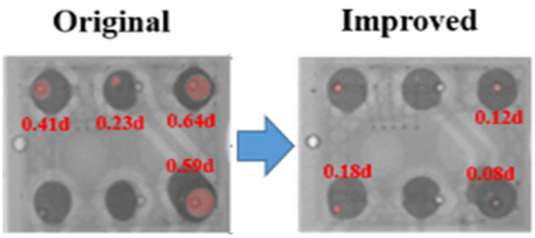

Fig. 6. Soldering defects(void) improvement

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