

Applying the I-V Method and the Dynamic Sampling to Implement Complex Impedance Measurement in A Hybrid ARM-FPGA based Platform

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ABSTRACT

This paper presents the use of a novel hybrid ARM-FPGA platform to design a complex impedance measurement system with the I-V method and the dynamic sampling rate. The system uses a programmable and fully integrated direct digital synthesis (DDS) chip to generate a stable sine wave and be applied to a complex impedance measurement circuit. Two 256-point Fast Fourier Transform (FFT) Hardware Description Language (HDL) modules are implemented in the FPGA to reduce the computing burden on the ARM processor and improve its performance. The dynamic sampling technique is used to reduce the leakage effect of the FFT, which applies a 200 MHz sampling counter to dynamically and precisely adjust the sampling frequency of ADC according to the output frequency of the DDS. Finally, the ARM processor inside the FPGA reads the magnitude and phase information of voltages $V_1(t)$ and $V_2(t)$ from the 256-point FFT HDL modules, respectively, and then calculates the magnitude and phase of the Z_{DUT} based on the R_{REF} .

Keywords: impedance measurement, I-V method, fast fourier transform, dynamic sampling

應用電流電壓法與動態取樣實現複數阻抗量測在 混合 ARM-FPGA 平台

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摘 要

本文以混合 ARM-FPGA 為核心的平台採用電流電壓方法與動態取樣率，設計複數阻抗量測系統。使用可程式的數位訊號合成晶片產生穩定的正弦波，加在複數阻抗量測電路上。以 FPGA 實現兩個獨立的 256 點的快速傅立葉轉換模組，可減少 ARM 處理器的運算負荷，並有效提昇效能。以 200 MHz 的取樣計數器動態且精確地依照正弦波的輸出頻率，調整數位類比轉換器的取樣時間，動態取樣技術可減少使用快速傅立葉轉換時會產生的洩漏效應。最後以在 FPGA 內部的 ARM 處理器，分別讀取由兩個 256 點的快速傅立葉轉換模組，所計算出的 $V_1(t)$ 與 $V_2(t)$ 的振幅與相位。再以參考電阻計算並求出未知複數電阻的大小與相位。

關鍵詞：阻抗量測，電流-電壓法，快速傅立葉轉換，動態取樣

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I. INTRODUCTION

Impedance measurement is a fundamental technique with applications in various fields, such as biomedical applications [1], electrochemistry [2], piezoelectric material analysis and applications [3], etc. However, a commercial impedance analyzer is quite expensive and not affordable for general companies or research institutes. Therefore, in recent years, many studies have been proposed which design a simplified impedance measurement system with a microcontroller or digital signal processor (DSP) to improve the accuracy and performance of the impedance measurement system at an acceptable cost [4-5]. However, the microcontroller/digital signal processor has to devote a great deal of its performance capability to handshake with the ADC and execute computations with the Fast Fourier Transform (FFT) or the sine fitting algorithm to obtain amplitude and phase information from the converted digital data of ADC. Additional factors also limit the development of the impedance measurement system, such as the range of measurement frequency, the accuracy of impedance, the friendly graphical user interface, internet of things (IoT) applications, etc.

A hybrid ARM-FPGA is a novel product developed in recent years which is integrated into a dual core ARM Cortex-A9 processor inside the FPGA. As is widely recognized in the industry, the FPGA can use internal logic cells to synthesize a variety of arbitrary digital hardware modules by written HDL according to design requirements; these synthesis hardware modules can work in parallel as well as independent of each other. The characteristics of the FPGA make it very suitable to handshake with two independent ADCs via general purpose input/output (GPIO) pins to simultaneously acquire and convert two analog signals from the measurement circuit to digital data. The digital data are then calculated with two independent 256-point FFT HDL modules to obtain the amplitude and phase information. The ARM processor is a high performance and 32-bit processor widely used in embedded systems such as mobile phones, tablets, digital cameras, portable electronic products, etc. The embedded Linux is the most commonly used operating system for ARM processors. It is very suitable for developing the friendly graphic user interface (GUI) and internet applications for the impedance measurement system.

Therefore, the complex impedance measurement system will apply the characteristics and advantages of the FPGA and the ARM processor to design with a hybrid ARM-FPGA platform. At the end of the paper, a commercial LCR meter will be used to verify the impedance measurement equipment presented in this paper.

II. MEASUREMENT METHODOLOGY

2.1 The Measurement Circuit of the I-V Method

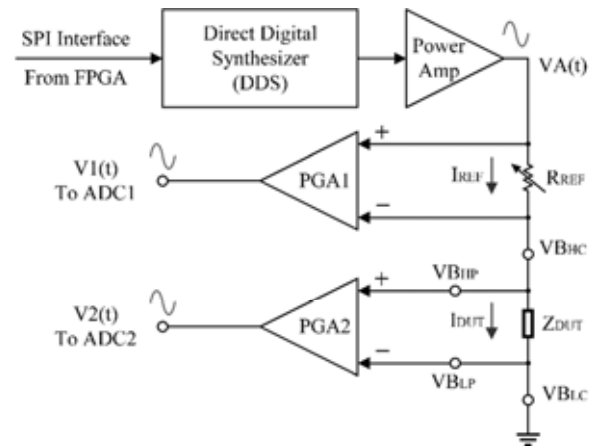


Fig. 1(a). The four-terminal (4T) configuration

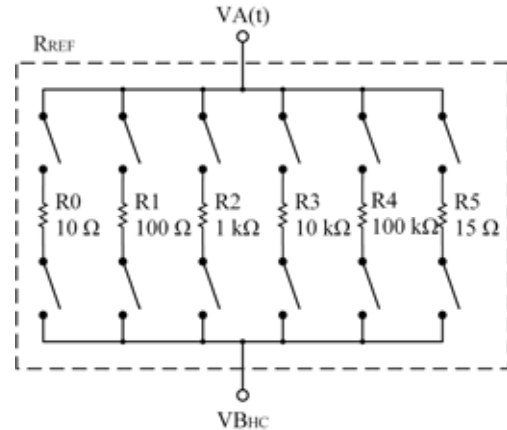


Fig. 1(b). The Relay-Based Reference Resistor (R_{REF}) Select Circuit

There are many measurement methods which can be used to measure the magnitude and phase of an unknown impedance Z_{DUT} , with each method having advantages and disadvantages. In this paper, the impedance measurement system applies the familiar Ohm's law to obtain impedance from the Z_{DUT} , a system hereafter

designated as the I-V method [6].

Fig. 1(a) and (b) show the measurement circuit of the I-V method. It uses a four-terminal configuration (VB_{HC} , VB_{HP} , VB_{LP} and VB_{LC}) to connect the unknown impedance Z_{DUT} ; this can effectively reduce the effect of lead impedances. The Direct Digital Synthesizer (DDS) outputs a stable sine wave $VA(t) = \sin(2\pi F_a t)$ and can modify the output frequency F_a via the digital SPI interface from the FPGA. The R_{REF} is selected by a relay-based reference resistor select circuit composed of 6 pure resistors (10 Ω , 100 Ω , 1 k Ω , 10 k Ω , 100 k Ω and 15 Ω) and 6 double pole double throw (DPDT) relays, as shown in Fig. 1(b). The PGA1 and PGA2 are the programmable gain instrumentation amplifiers (PGA) which can modify the gain via the digital signals from the FPGA.

According to Ohm's law, the unknown impedance Z_{DUT} is the ratio of the voltage across the Z_{DUT} to the current flows of the Z_{DUT} , as represented in formula (1).

$$Z_{DUT} = \frac{VB_{HP} - VB_{LP}}{I_{DUT}} \quad (1)$$

and

$$I_{DUT} = I_{REF} = \frac{VA - VB_{HC}}{R_{REF}} \quad (2)$$

Substitute formula (2) into formula (1)

$$Z_{DUT} = \frac{VB_{HP} - VB_{LP}}{VA - VB_{HC}} \times R_{REF} \quad (3)$$

and

$$\begin{aligned} VB_{HP} - VB_{LP} &= \frac{V2}{GAIN_{PGA2}} \\ VA - VB_{HC} &= \frac{V1}{GAIN_{PGA1}} \end{aligned} \quad (4)$$

Where $GAIN_{PGA1}$ represents the gain of PGA1, and $GAIN_{PGA2}$ gives the gain of PGA2.

$$Z_{DUT} = \frac{V2}{V1} \times \frac{GAIN_{PGA1}}{GAIN_{PGA2}} \times R_{REF} \quad (5)$$

In order to calculate the complex impedance, formula (5) denotes as formula (6)

$$Z_{DUT} = \frac{|V2|\angle\theta_2}{|V1|\angle\theta_1} \times \frac{GAIN_{PGA1}}{GAIN_{PGA2}} \times R_{REF} \quad (6)$$

where $|V1|$ and $|V2|$ represent the amplitudes (peak voltages) of $V1(t)$ and $V2(t)$, respectively, while the $\angle\theta_1$ and $\angle\theta_2$ represent the phases of $V1(t)$ and $V2(t)$, respectively.

Finally, the Z_{DUT} denotes as the polar form, as represented in formula (7).

$$Z_{DUT} = \left(\frac{|V2|}{|V1|} \cdot \frac{GAIN_{PGA1}}{GAIN_{PGA2}} \cdot R_{REF} \right) e^{j(\angle\theta_2 - \angle\theta_1)} \quad (7)$$

$$\begin{aligned} |Z_{DUT}| &= \frac{|V2|}{|V1|} \cdot \frac{GAIN_{PGA1}}{GAIN_{PGA2}} \cdot R_{REF} \\ \angle Z_{DUT} &= \angle\theta_2 - \angle\theta_1 \end{aligned} \quad (8)$$

where the $|Z_{DUT}|$ represents the magnitude of the Z_{DUT} , and $\angle Z_{DUT}$ gives the phase of the Z_{DUT} .

The amplitudes and phases of $V1(t)$ and $V2(t)$ can calculate by the Fast Fourier Transform (FFT) algorithm, and then apply formula (8) to compute the Z_{DUT} .

2.2 Applying Dynamic Sampling to Fast Fourier Transform

Fast Fourier Transform (FFT) is an algorithm which can convert a periodic sequence of the time domain into the frequency domain to get the magnitude and phase information at distinct frequencies. It is a mature technology for the implementation of the FFT algorithm in an FPGA [7]. Thus, the FPGA will integrate two 256-point FFT with radix-2 HDL modules to get the amplitude and phase information from $V1(t)$ and $V2(t)$, respectively.

However, the aliasing effect and spectral leakage are common issues when using the FFT algorithm [8]. To avoid the aliasing effect, two anti-aliasing filters can place in front of two ADCs (for the $V1(t)$ and $V2(t)$ signals).

In the impedance measurement circuit, the DDS outputs a single sine wave $VA(t)$ with a frequency of F_a . To avoid spectral leakage, the sampling frequency F_s must be an integer multiple of F_a and denote the multiple as M_1 . Moreover, M_1 represents the number of sampling points per period of $V1(t)$ and $V2(t)$. As such, M_1 must also be a power of two for the radix-2 FFT algorithm.

$$\frac{F_s}{F_a} = M_1 \text{ for } M_1 = 2, 4, 8, 16, \dots \quad (9)$$

Therefore, the dynamic sampling scheme will adopt the characters of FPGA to implement for signal acquisition, which means the sampling frequency F_s will be dynamically and automatically adjusted with the signal frequency

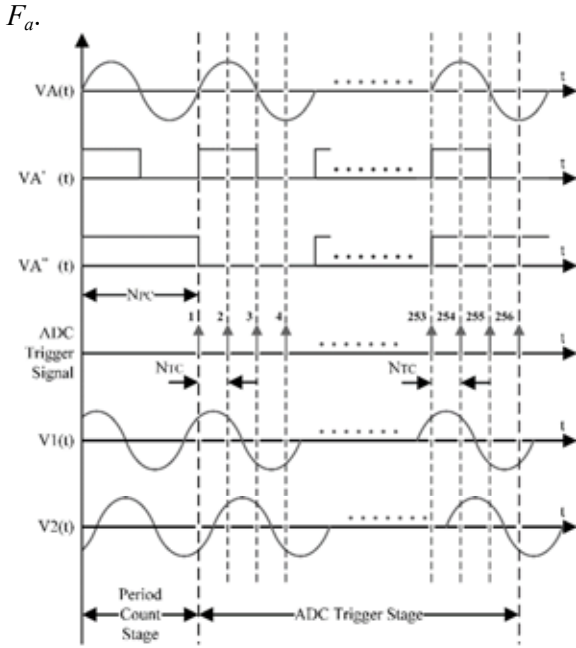


Fig. 2(a). The Dynamic Sampling Operational Scheme

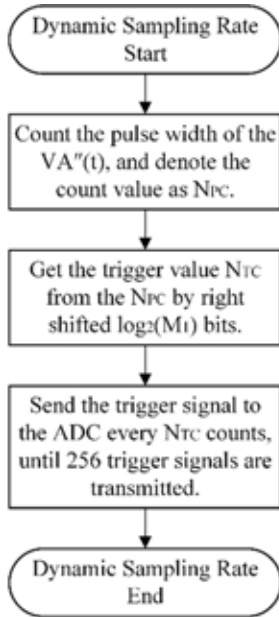


Fig. 2(b). The Dynamic Sampling Operational Flowchart

As shown in Fig. 2, $VA(t)$ is the output signal of the DDS, and $VA'(t)$ is the sign bit of the DDS—the logic voltage level. The sign bit $VA'(t)$ is directly connected into a flip-flop inside the FPGA via the I/O pin of the FPGA. The signal $VA''(t)$ is the output signal of the flip-flop inside the FPGA. The pulse width of the $VA''(t)$ is the same as the period of $VA(t)$. A high-speed counter inside the Sampling Trigger HDL module to count the pulse width of $VA''(t)$

and generate the trigger signals for two ADCs. The N_{PC} is the count value of the period of $VA(t)$, and the N_{TC} is the count value between two trigger signals. In the period count stage, the Sampling Trigger HDL module uses the high-speed counter to count the pulse width of $VA''(t)$ to get the count value N_{PC} . When the M_1 equals 4, it means that there are four sampling points per period of the $VA(t)$. Thus, N_{TC} is N_{PC} divided by 4. Furthermore, when M_1 equals 8, it means that there are eight sampling points per period of the $VA(t)$. It becomes evident that N_{TC} is N_{PC} divided by 8, and so on. The FPGA can apply a simple bit shift operation to get the N_{TC} from the binary format of the N_{PC} . For example, when the N_{PC} equals 1024 (0100 0000 0000b) and M_1 equals 4, N_{TC} represents the binary format of the N_{PC} shifting two places to the right. As such, N_{TC} equals 256 (0001 0000 0000b). Following this pattern, when the N_{PC} equals 1024 (0100 0000 0000b) and the M_1 equals 8, the N_{TC} represents the binary format of the N_{PC} shifting three places to the right. Thus, the N_{TC} equals 128 (0000 1000 0000b). The dynamic sampling scheme has a rounding error which increases with increasing the sampling rate, but decreases with increasing the frequency of the counter inside the Sampling Trigger HDL module. Spectral leakage can be eliminated when an integer number of periods of a signal are sampled by the ADC. The high-frequency counter inside the Sampling Trigger HDL module can accurately send the trigger signals to the ADC every N_{TC} counts, to more completely match the actual signal and to reduce the spectral leakage effect of FFT.

The ADC trigger stage starts at the rising edge of the sign bit $VA'(t)$; the Sampling Trigger HDL module outputs 256 trigger signals for two ADCs to convert signals $V1(t)$ and $V2(t)$, and the 256 trigger signals are separated from each other by the N_{TC} . As shown in Fig. 2(a), sampling rate F_s of the ADC will dynamically and automatically adjust according to frequency F_a of the $VA(t)$ and the multiple M_1 , which can effectively reduce spectral leakage in the FFT algorithm.

III. SYSTEM IMPLEMENTATION

3.1 System Architecture

Fig. 3 shows the block diagram (top) and the clock distribution (bottom) of the hybrid ARM-FPGA based impedance measurement platform. U1 is a 32-bit high-performance ARM Processor inside the FPGA, which runs an embedded

Linux system and performs the following tasks: firstly, receives user commands/sends impedance measurement data via the TCP/IP network interface; next, sets the specified output

frequency of the DDS via the SPI interface; and finally enables the FFT Controller HDL module and receives the FFT data of $V_1(t)$ and $V_2(t)$ to calculate the unknown impedance Z_{DUT} .

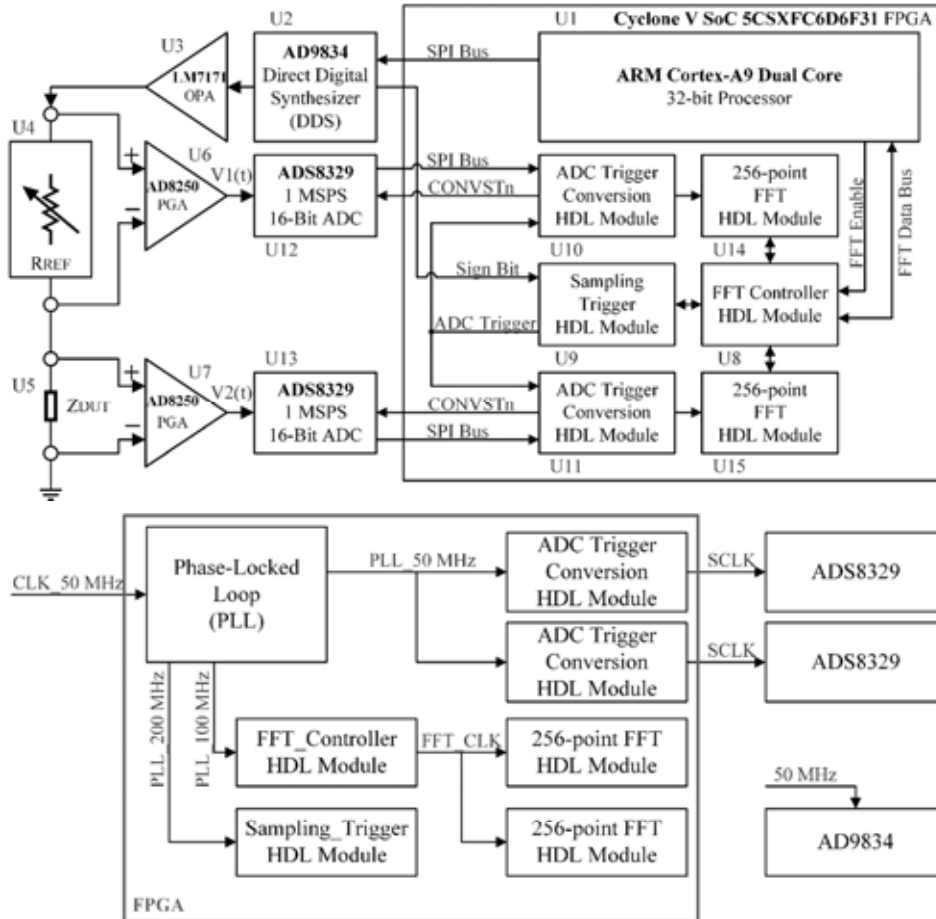


Fig. 3. The Block Diagram (top) and the Clock Distribution (bottom) of a Hybrid ARM-FPGA based Complex Impedance Measurement Instrument

U2 is a Direct Digital Synthesizer (DDS) chip which can modify the internal 28-bit frequency register ($FREQ_REG_{28bit}$) to output the specified frequency of the sine wave to the power amplifier. The f_{MCLK} is a crystal oscillator which provides the clock source to the DDS. $FREQ_REG_{28bit}$ is the internal frequency register which can modify via the SPI interface of the DDS. The output frequency of the DDS can be calculated by formula (10):

$$\text{The DDS Output Frequency} = \frac{f_{MCLK}}{2^{28}} \times FREQ_REG_{28bit} \text{ Hz} \quad (10)$$

U3 is a power amplifier which can enable the DDS output signal to have enough power to drive the impedance measurement circuit. U4 is a relay-based reference resistor select circuit

which can use the relay to switch the optimal R_{REF} channel according to the magnitude of the Z_{DUT} . U5 is the unknown impedance device under the test Z_{DUT} . U6 and U7 are the programmable gain instrumentation amplifiers (PGA) which can amplify the voltage signal from the R_{REF} and the Z_{DUT} ; the gain of the amplifiers can be controlled by the digital interface of the PGA. The output voltage of PGA1 is denoted as $V_1(t)$, and the output voltage of PGA2 is denoted as $V_2(t)$. U8 is an FFT controller HDL module which can receive commands from the ARM processor and enables the Sampling Trigger HDL module to work, obtaining the FFT converted data from the 256-point FFT HDL module and then sending the data to the ARM processor. U9 is the Sampling Trigger HDL module which can receive the sign bit signal (Sign Bit) of the sine wave from the

DDS and calculate the trigger interval time, subsequently sending the ADC trigger signal (ADC Trigger) to the ADC Trigger Conversion HDL module. U10 and U11 are the ADC Trigger Conversion HDL modules which receive the ADC trigger signal (ADC Trigger) from the Sampling Trigger HDL module, sending the ADC converted trigger signal (CONVSTn) to the Analog-to-Digital Converter and then receiving the converted data via the SPI interface (SPI Bus). U12 and the U13 are the 1 MSPS 16-bit ADCs which can convert the analog voltages from PGA1 and PGA2 to the digital data, respectively. U14 and U15 are the hardware 256-point FFT HDL modules which can implement the FFT algorithm independently without consuming the performance of the ARM processor inside the FPGA. The calculated results of the 256-point FFT HDL modules are then sent to the ARM processor via the FFT Controller HDL module. Finally, the ARM processor receives the operation results of the FFT Control HDL modules which include the real number and imaginary number of $V_1(t)$ and the $V_2(t)$, and can calculate the magnitude and phase of the Z_{DUT} by formula (8). Although the multiple sets of different clocks (50 MHz, 100 MHz and 200 MHz) are used in this system. They are all generated from the same PLL, and each HDL module uses only one clock source to avoid the metastability. For example, the ADC Trigger Conversion HDL modules are driven by a 50 MHz. The FFT_Controller HDL module and the 256-FFT HDL modules are driven by a 100 MHz. The Sampling_Trigger HDL Module is driven by a 200 MHz. Fig. 4 shows the top view of the hybrid ARM-FPGA based complex impedance measurement instrument.

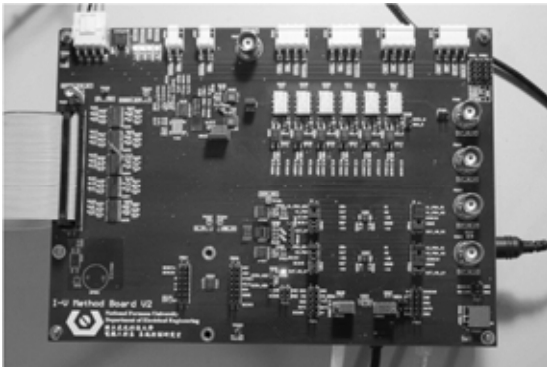


Fig. 4. The Hybrid ARM-FPGA based Complex Impedance Measurement Instrument

3.2 Calibration and Compensation

Before starting the impedance measurement experiment, the impedance measurement system

needs to be calibrated and compensated to improve its accuracy. Fig. 5(a) shows the 6 precision resistors ($R_{CALIBRATION}$) for calibrating the 6 reference resistors (R_{REF}) in our system.

Due to the fact that the values of the precision resistors ($R_{CALIBRATION}$) are known, the impedance of the reference resistors can be calculated by formula (11).

$$R_{REF} = \left(\frac{|V_1| \angle \theta_1}{|V_2| \angle \theta_2} \right) \left(\frac{GAIN_{PGA2}}{GAIN_{PGA1}} \right) R_{CALIBRATION} \quad (11)$$

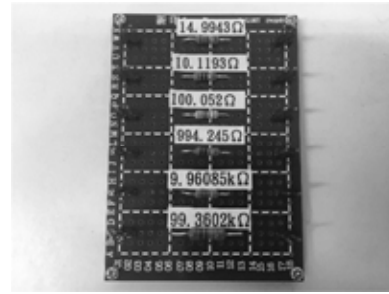


Fig. 5(a). The Calibration Resistors

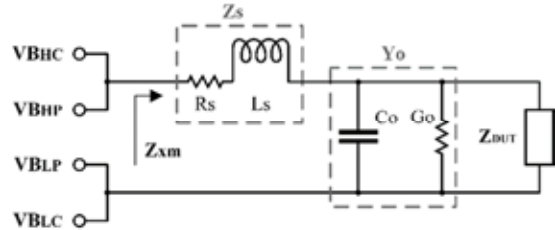


Fig. 5(b). The Residual Impedance Z_s and the Stray Admittance Y_o

Furthermore, there are residual impedance (Z_s) and stray admittance (Y_o) in the impedance measurement circuit as shown in Fig. 5(b) which influence the accuracy of the impedance measurement system. The OPEN and SHORT compensation method will be used to minimize errors.

Z_{xm} is the measured impedance of the Z_{DUT} when Z_s and Y_o exist in the impedance measurement circuit. Y_o can be measured when the probe is open and Z_s when the probe is short.

In the ARM-Linux operational system, Y_o and Z_s measured at different frequencies can be saved as a calibration file. When Z_{xm} is measured at the specified frequency, the ARM processor can find the corresponding Y_o and Z_s from the calibration file according to the current measurement frequency; and calculate the Z_{DUT} using formula (12).

$$Z_{DUT} = \frac{Z_{xm} - Z_s}{1 - (Z_{xm} - Z_s)Y_o} \quad (12)$$

Fig. 6 shows Z_{xm} and the Z_{DUT} for the 10 k Ω pure resistor measurement, and the measurement frequency from 1 kHz to 50 kHz. Due to the existence of Z_s and Y_o , the errors of the magnitude and the phase of Z_{xm} are large with frequency. The errors of the magnitude and the phase of the compensated measurement impedance Z_{DUT} are both significantly lower than those of Z_{xm} .

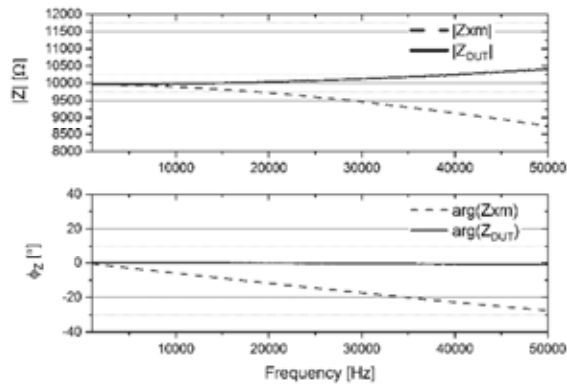


Fig. 6. The Z_{xm} and the Z_{DUT} vs. Frequency

IV. EXPERIMENTAL RESULTS

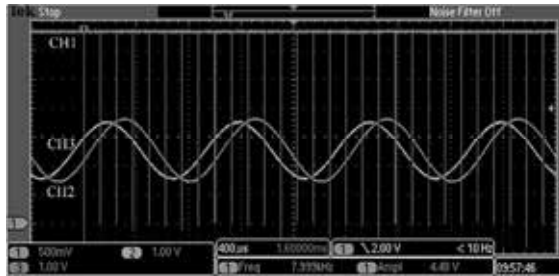


Fig. 7(a). The Impedance Measurement Waveforms (the V1 and the V2) with the Dynamic Sampling Trigger Signal

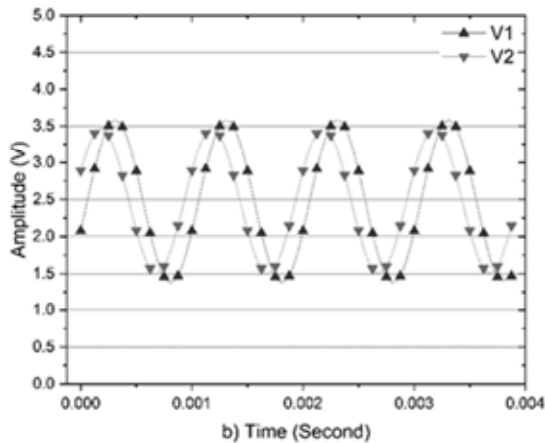


Fig. 7(b). The ADC Sampling Waveforms of the V1 and the V2 ($M_1=8$)

Fig. 7(a) shows the measurement signals of the Z_{DUT} as measured by the Tektronix MSO2024B oscilloscope when parameter $M_1=8$. M_1 can be set to 8, 16, 32 or 64 by the ARM Processor (Set $M_1=8$ in this paper). When $M_1=8$, this means every cycle has eight sampling points. On the screen of the oscilloscope, CH1 is the conversion trigger signal (the falling edge) of the ADC automatically produced from the ADC Trigger Conversion HDL module and the Sampling Trigger HDL module inside the FPGA according to the output frequency of the DDS. This is the dynamic sampling function in our impedance measurement system. CH2 is the V1(t) signal from the PGA1 and CH3 is the V2(t) from PGA2. It can be known that every cycle has 8 sampling points in the V1(t) and V2(t) signals in Fig. 7(a). In Fig. 7(b), the triangle symbols “ $\blacktriangle$ ” and “ $\blacktriangledown$ ” represent the ADC sampling and converted data of V1(t) and V2(t), respectively.

In order to verify the impedance measurement system as proposed in this paper, the 6 impedance samples have measured with the GW INSTEK LCR-6300 LCR Meter to obtain the standard value of the impedance samples Z_{STD} . Table 1 shows the magnitudes and phases of the 6 impedance samples measured at the frequencies of 1 kHz and 10 kHz.

The output frequency of the DDS is calculated by formula (10) and f_{MCLK} was 50 MHz in the impedance measurement system. Therefore, the $FREQ_REG_{28bit}$ can set to 5368 (14F8H) and 53687 (D1B7H) to obtain the DDS output frequency of 999.868 Hz and 9999.983 Hz, respectively. Fig. 8 shows the 1000 repeated 999.868Hz impedance measurements for the 6 samples, and the Fig. 9 shows the 1000 repeated 9999.983 kHz impedance measurements for the 6 samples. Table 2 shows the 1000 repeated experimental results of the 6 samples test with our impedance measurement system at frequencies of 999.868 Hz and 9999.983 Hz, respectively.

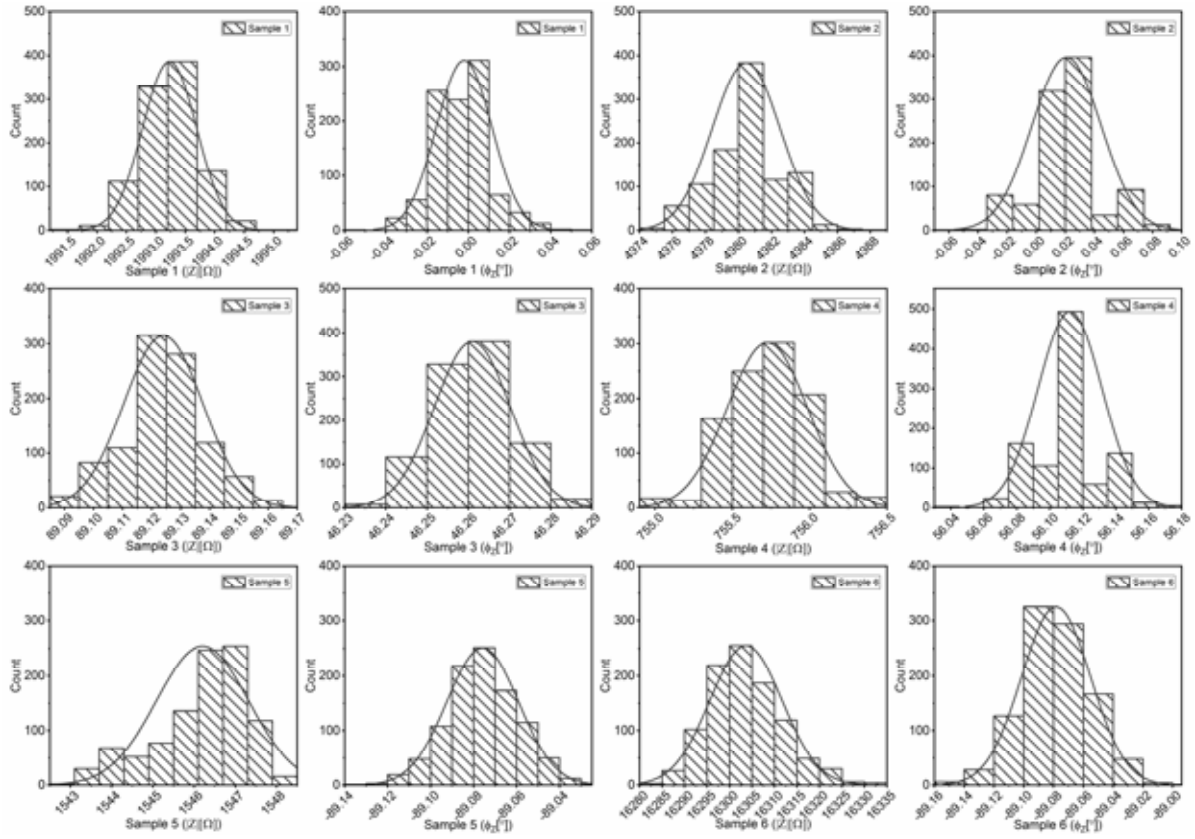


Fig. 8. The 1000 Repeated 999.868Hz Impedance Measurements for the 6 Samples

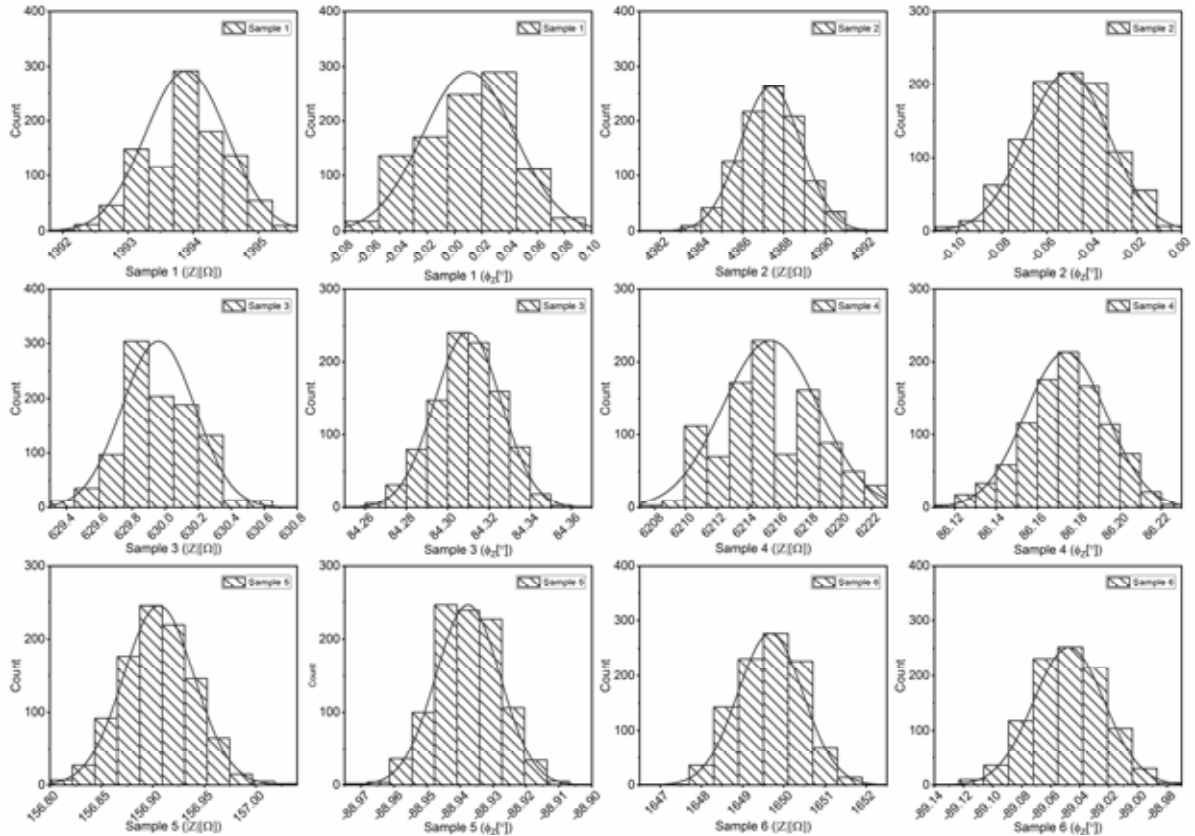


Fig. 9. The 1000 Repeated 9999.983Hz Impedance Measurements for the 6 Samples

Table 2. 1000 Times Average Measurement Results for the 6 Impedance Samples

Sample (DUT)	Frequency	$ Z $	Z_θ	$\frac{\sigma_{ Z }}{ Z }$	σ_{Z_θ}	Relative Error $ Z $	Absolute Error Z_θ
	[Hz]	[Ω]	[$^\circ$]	%	[$^\circ$]	%	[$^\circ$]
1	999.868	1993.23	-0.002	0.0231%	0.01353	0.0045%	0.0046
	9999.983	1993.89	0.0103	0.0314%	0.03340	0.0386%	0.0046
2	999.868	4980.46	0.0208	0.0415%	0.02376	0.0092%	0.0186
	9999.983	4987.36	-0.0507	0.0296%	0.01829	0.1281%	0.0508
3	999.868	89.12	46.261	0.0151%	0.00924	0.7849%	0.048
	9999.983	629.96	84.3098	0.0349%	0.01614	0.8218%	0.0788
4	999.868	755.73	56.1122	0.0342%	0.01952	0.5029%	0.0352
	9999.983	6215.46	86.1737	0.0499%	0.01971	0.0505%	0.1327
5	999.868	1546.2	-89.0758	0.0728%	0.01674	0.3179%	0.0662
	9999.983	156.91	-88.9376	0.0221%	0.00981	0.6543%	0.0234
6	999.868	16303.65	-89.0783	0.0495%	0.02330	0.2191%	0.0987
	9999.983	1649.67	-89.0475	0.0481%	0.02440	0.1804%	0.0225

Table 1. Test 6 Impedance Samples with a GW INSTEK LCR-6300 LCR Meter

Samples	Frequency	$ Z_{STD} $	$Z_{STD\theta}$
	[kHz]	[Ω]	[$^\circ$]
1	1	1993.14	0.0026
	10	1993.12	0.0057
2	1	4980.92	0.0022
	10	4980.98	0.0001
3	1	89.825	46.309
	10	635.18	84.231
4	1	759.55	56.077
	10	6218.6	86.041
5	1	1541.3	-89.142
	10	155.89	-88.961
6	1	16268	-89.177
	10	1646.7	-89.07

V. CONCLUSIONS

This paper proposes applying the I-V method to implement impedance measurement in a hybrid ARM-FPGA based platform with a dynamic sampling rate. FPGA is responsible for precisely sending the convert trigger signal to the two ADCs according to the output frequency of the DDS automatically, reading the converted data from the two ADCs via the SPI interface, and implementing the hardware 256-point FFT algorithms to attain the real and imaginary number from the converted data of the two ADCs. The ARM processor of the inside the FPGA is responsible for receiving the FFT data from the FFT Controller HDL module and implementing complex number operations to obtain the magnitude and phase of the Z_{DUT} using the above formulas.

The 6 samples are tested with the impedance measurement system for 1000 repeated experiments at frequencies of both 999.868 Hz and 9999.983 Hz; table 2 shows the experimental results. The symbol $|Z|$ denotes the mean of the magnitude of the impedance sample for the 1000 repeated measurements. The symbol Z_θ denotes the mean of phase of the impedance sample for the 1000 repeated measurements. The symbol $\sigma_{|Z|}/|Z|$ is the standard deviation of the magnitude of the impedance sample divided by the mean of the magnitude of the impedance sample; the unit of the symbol is a percentage. The symbol σ_{Z_θ} is the standard deviation of the phase of the impedance sample. The relative error $|Z|$ represents the absolute value of the $(|Z| - |Z_{STD}|)$ divided by $|Z_{STD}|$; its unit is a percentage. The absolute error Z_θ represents the absolute value of the $Z_\theta - Z_{STD}$.

According to the experimental results, although some histograms show slight skew, such as the sample 5 in the Fig. 8 and sample 3 in the Fig. 9. But it can be known that each $\sigma_{|Z|}/|Z|$ is below 0.1%, and each σ_{Z_θ} is below 0.1 degrees from the table 2. The low standard deviation represents the fact that the 1000 repeated measurement results are close to the mean of the set. In other words, the results of the 1000 repeated impedance measurements are stable with our impedance measurement system. Relative and absolute errors are common approximation errors, meaning a discrepancy between the exact value and the measurement results. The low approximation error represents the fact that the measurement results are close to the exact value. Table 2 shows that the minimum

relative error $|Z|$ is 0.0045% and the maximum relative error $|Z|$ is 0.8218%. The minimum absolute error Z_0 is 0.0046 degrees and the maximum absolute error Z_0 is 0.1327 degrees.

From the above experimental results, it can be known that due to the characteristics of the I-V method in addition to the influence of the residual impedance (Z_s) and the stray admittance (Y_o), the accuracy of the impedance measurement still needs to improve, especially in the high measurement frequency and high magnitude of Z_{DUT} .

Impedance measurement is a very basic but important electrical measurement function. Therefore, some manufacturers design the components required for impedance measurement in a single chip. For example, AD5933 chip launched by Analog Device.

The main advantage of using an impedance conversion chip for design is that it can greatly simplify the design circuit and reduce the time required for program development.

But its disadvantage is that it is difficult to modify the design according to actual needs.

Table 3 shows the comparison of the impedance measurement characteristics based on the hybrid ARM-FPGA platform and the AD5933. When the more precise measurement is required, it is difficult to change the 12-bit ADC in AD5933 to a 16-bit ADC.

Table 3. Comparison of the impedance measurement characteristics based on the hybrid ARM-FPGA platform and the AD5933

	A Hybrid ARM-FPGA based Platform	AD5933 (Analog Device)
Measurement Method	I-V Method	ABB Method (Auto-balancing bridge method)
Impedance Range	10 Ω To 1 M Ω	100 Ω to 10 M Ω
ADC Resolution	16-Bit	12-Bit
Sampling Rate	1 MSPS	1 MSPS
Maximum Measurement Frequency	50 kHz	100 kHz

Finally, the prototype of the impedance measurement system was built with a hybrid ARM-FPGA based platform. Most works have been implemented by FPGA. In the future, the ARM processor inside the FPGA can build a

full-featured human-machine interface (HMI) for engineers to easily use in addition to developing a network communication and control function in the embedded Linux operating system for the ARM processor to apply on the production line.

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