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Study on Operation Performance of Flash Memory at High Temperature

Chia-Huai Ho[1*], Ching-Tung Lo[2], Han-Lin Hsiung[3]

[1]Department of Optometry, Kang Ning University, Taipei, Taiwan, R.O.C.
[2]Department of Computer and Communication Engineering, Army Academy, Taoyuan, Taiwan, R.O.C.
[3]Department of Business Administration, Kang Ning University, Taipei, Taiwan, R.O.C.
[*]Corresponding author: Tel:886-933-532016; E-mail address: jh.ho@msa.hinet.net

Abstract

In recent years, with the miniaturization of components, the limitations of packaging technology and the increase of component integration have increased. It will increase the operating temperature of the component, so the effect of temperature change on the performance of the flash memory is very important.

In this paper, firstly, the operation performance value of the flash memory experimental measurement is compared with the simulated performance value, and after obtaining the consistent performance trend, the simulated data is used to analyze and explain the difference in performance of the flash memory in the room temperature and high temperature environment.

The experimental analysis shows that when the temperature is higher, the threshold voltage shift between the measured and simulated flash memory writing and erasing operations becomes larger and larger. Moreover, the flash memory has a larger tunnel surface electric field value and higher electron injection probability at high temperature, so the operation performance is still better at high temperatures.

Index terms: flash, operation performance, MEDICI, threshold voltage shift, energy band diagram

I、INTRODUCTION

With the evolution of process technology and circuit layout, Flash Memory in read-only memory has received considerable attention in recent years. Compared with other types of memory, it contains considerable advantages and applications. Its application is also quite extensive, and it can be used in most portable electronic products, even in the aerospace industry. However, in the process of miniaturization of components, due to the limitations of packaging technology and the increase in component integration, the operating

temperature of the component will rise, so the temperature change can have significant effect on the performance of the flash memory. [1]

The currently published literature on the performance of flash memory in high temperature environment mostly focuses on the analysis and research of the performance of a certain feature of the component itself during component operation, for example: "Temperature Effect on Read Current In a Two-Bit Nitride-Based Trapping Storage Flash EEPROM Cell" [2] is to study the effect of temperature on the read operation performance of flash memory. "Stress-Induced Leakage Current of Tunnel Oxide Derived from Flash Memory Read-Disturb Characteristics" [3] is to analyze the difference in read-disturb performance of flash memory in room temperature and high temperature environments. However, few studies have extensively explored the performance of writing and erasing operations of flash memory in high temperature environments.

In this paper, the operating performance value of the actual flash memory measurement is compared with the simulated performance value to obtain a consistent performance trend, and then the simulated data is used to analyze and explain the flash memory in the room temperature and high temperature environments to show the difference in performance.

II、MEASUREMENT AND SIMULATION

In this paper, the actual measured flash memory is the n-type flash device with gate length(L) = 70nm, wherein N_{sub} = $2X10^{16}$ cm^{-3}, N_{source} = $7X10^{18}$ cm^{-3}, N_{drain} = $7X10^{18}$ cm^{-3}, and gate stack thickness is: control gate = 0.05 nm, top oxide = 0.013 nm, floating gate = 0.1 nm and bottom oxide = 0.009 nm. The programming biases are V_d = 5V, V_{cg} = 20V(gate coupling ratio is 0.6), V_s = 0V, V_{sub} = 0V, and the erasing biases are V_d = 0V, V_{cg} = -20V, V_s = 6V, V_{sub} = 0V.

The tool used for the simulation is the component electrical simulation software MEDICI [4], and the physical model used in the simulation, including: Concentration Dependent Mobility Model (CONMOB), Perpendicular Electric Field Mobility Model (PRPMOB), Field-Dependent Mobility Model (FLDMOB), Models such as Shockley-Read-Hall Recombination Model (CONSRH), Auger Recombination Model (AUGER) and Band-Gap Narrowing Model (BGN), the simulated flash memory is the n-type flash device with gate length(L) = 0.9um, N_{sub} = $6X10^{16}$ cm^{-3}, N_{source} = $2X10^{20}$ cm^{-3} , N_{drain} = $2X10^{20}$ cm^{-3}. The gate stack thickness is: control gate = 0.05 nm, top oxide = 0.04 nm, floating gate = 0.025 nm and bottom oxide = 0.01 nm. The programming biases are V_d = 5.5V, V_{cg} = 20V (gate coupling ratio assumed 1/5), V_s = 0V, V_{sub} = 0V, and the erasing biases are V_d = 0V, V_{cg} = -15V, V_s = 10V, V_{sub} = 0V.

The measurement experiment first measures the write rate of the write operation and the erase rate of the erase operation at 300 ^oK, 350 ^oK, and 400 ^oK, and then measures the write and erase operations of the component from 300 ^oK to 400 ^oK and form the graph of the threshold

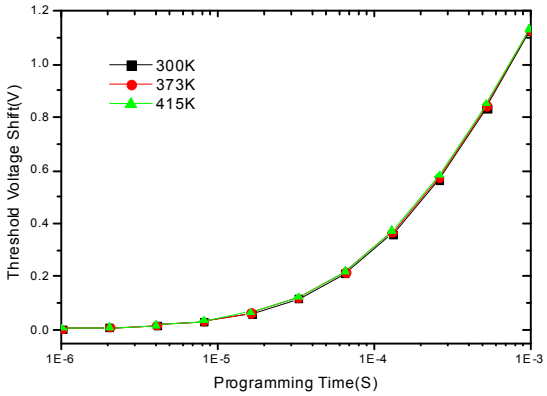
voltage along with temperature changes.

The simulation first simulates the write rate, write current, and surface injection current density value of the write operation at 300 ^{o}K, 373 ^{o}K, and 415 ^{o}K through the simulation software, as well as the erase rate and erase current of the erase operation and the surface erase current density value. Then, analyze the graph of the threshold voltage along with temperature changes during 300 ^{o}K to 415 ^{o}K component writing and erasing operations. It is compared with the measured data to observe the operating performance trend of the flash memory at high temperatures.

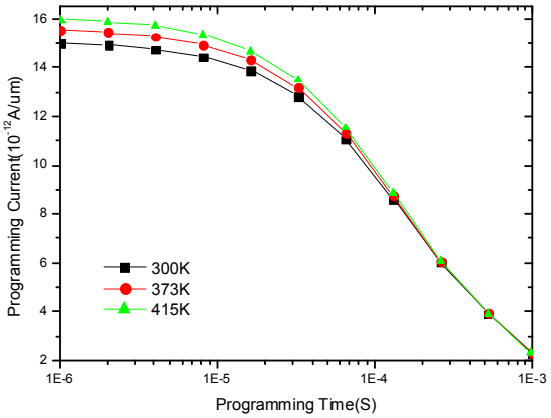
Finally, through the simulation of 300 ^{o}K, 373 ^{o}K and 415 ^{o}K components write operations, the electric field and electron injection probability comparison graph and potential graph of the 1D depth from the oxide and substrate junctions at 1.23um in the lateral position near the drain. Thus, it analyzes and explains the difference in writing and erasing performance of flash memory under high temperature operation. The 1.23um lateral position near the drain is taken because it is just the end of the junction between the component tunnel and the drain depletion region, which is exactly where the incident electron is injected and has a comparatively large probability of electron injection.

III、RESULTS AND DISCUSSION

Fig.1 is a comparison of the (a) write rate, (b) write current, and (c) surface injection current density of the simulated flash memory write operation at 300 ^{o}K, 373 ^{o}K, and 415 ^{o}K respectively. The programming biases are V_d = 5.5V, V_{cg} = 20V (gate coupling ratio assumed 1/5), V_s = 0V, V_{sub} = 0V. As can be seen from Fig. 1 (a), the writing rate at high temperature is slightly increased compared to room temperature. It can also be seen from Fig. 1 (b) and (c) that the performance of write current and the surface injection current density at high temperatures are also higher than those at room temperature. This is because the temperature rise increases the tunnel surface electric field value and the electron injection probability, and the number of electrons injected into the floating gate increases, and the result can be verified by the following simulation data.



(a)



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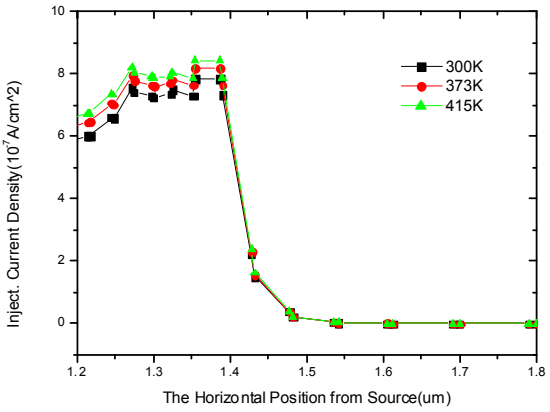
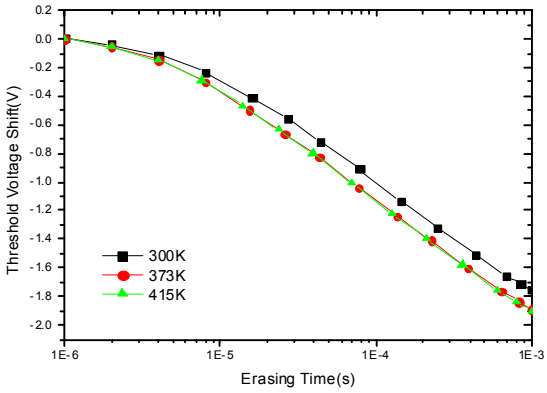


(c)

Figure 1 Comparison of (a) write rate, (b) write current, and (c) surface injection current density for simulated flash memory write operations at 300 ^{o}K, 373 ^{o}K, and 415 ^{o}K.

Fig. 2 is a comparison of (a) erasing rate, (b) erasing current, and (c) surface erasing current density of the simulated flash memory erase operation at 300 ^{o}K, 373 ^{o}K, and 415 ^{o}K. The erasing biases are V_d = 0V, V_{cg} = -15V, V_s = 10V, V_{sub} = 0V. As can be seen from Fig. 2(a), the erasing rate at high temperatures is higher than that at room temperature. It can also be seen from Fig. 2(b) and (c) that the erase current and the surface erase current density at high temperatures are also higher than those at room temperature. This is because the increase in temperature causes an increase in the electron heat emission in the floating gate, which in turn increases the number of electrons flowing out of the floating gate.



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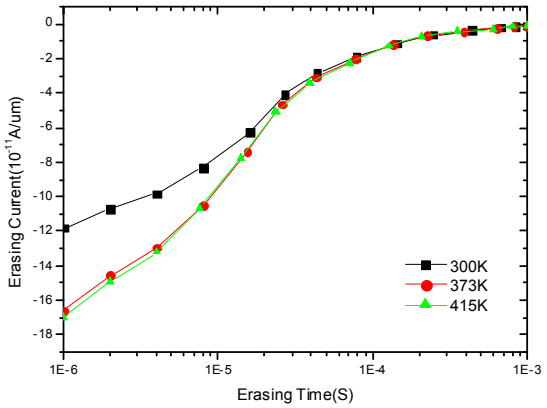

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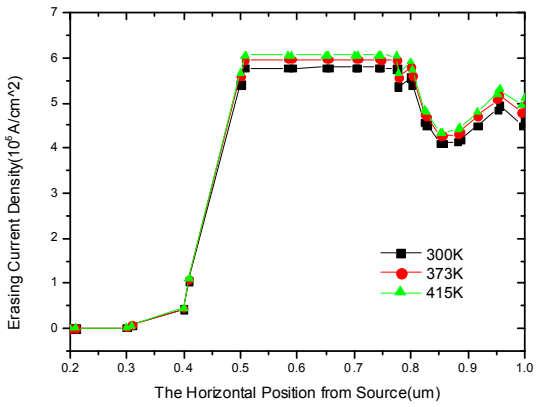
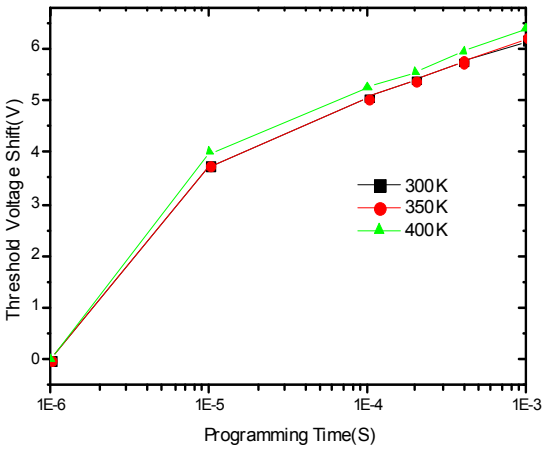


(c)

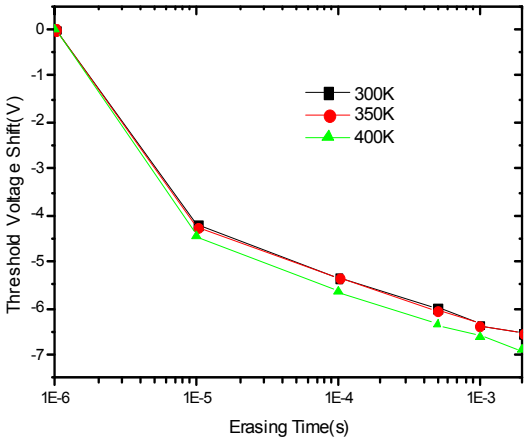
Figure 2 Comparison of (a) erase rate, (b) erase current, and (c) surface erase current density for simulated flash memory erase operations at 300 ^{o}K, 373 ^{o}K, and 415 ^{o}K.

This study also performed experimental measurements. Fig.3 shows the (a) write rate and (b) erase rate graph of the flash memory at 300 ^{o}K, 350 ^{o}K, and 400 ^{o}K. In Fig. 3(a),

the write rate performance of 300 °K and 350 °K is indistinguishable. However, as the ambient temperature rises, it can be seen that the writing speed of the flash memory at high temperatures is higher than at room temperature. In Fig. 3(b), the erase rate of 300 °K and 350 °K is insignificant. However, as the ambient temperature rises, it can be seen that the erasing rate of the flash memory at high temperatures is higher than at room temperature. Through the comparison of the above three figures, the write rate and erase rate performance trends of the simulated flash memory shown in Fig. 1 and Fig. 2 are similar to those of the flash memory write and erase rate performances measured in Fig. 3, and the current input, surface injection current density, erase current and surface erase current density curve of the simulated flash memory are also consistent with the write and erase rate performance trends, indicating that the simulation results of this paper should be correct.



(a)



(b)

Figure 3 Graph of experimentally measured (a) write rate and (b) erase rate of flash memory at 300 °K, 350 °K, and 400 °K.

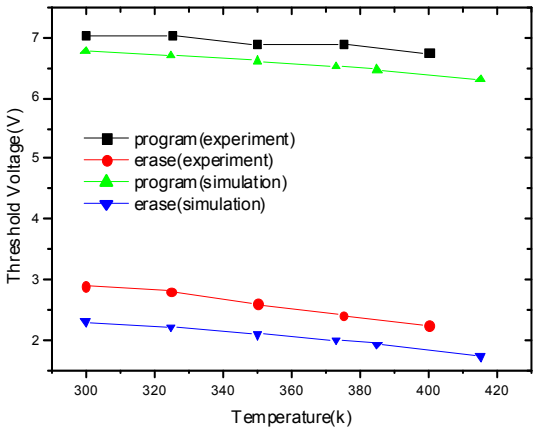
Fig. 4(a) is a comparison of the threshold voltages of the flash memory writing and erasing operations of the experimental measurement and simulation at different temperatures (300 to 415 °K). From this figure, it can be seen that when the temperature rises, the threshold voltage of the write operation of the simulated flash memory is consistent with the trend of temperature change, which has a variation of -4mV/°c to -2mV/°c. When the erase operation is performed, the threshold voltage of the measured and simulated flash memory is also changed by the above data. According to the following threshold voltage equation, we learned that,

$$V_T \fallingdotseq V_{FB} + 2\Psi_B + (2\varepsilon_S q N_A(2\Psi_B + V_{BS}))^{0.5} / C_O$$

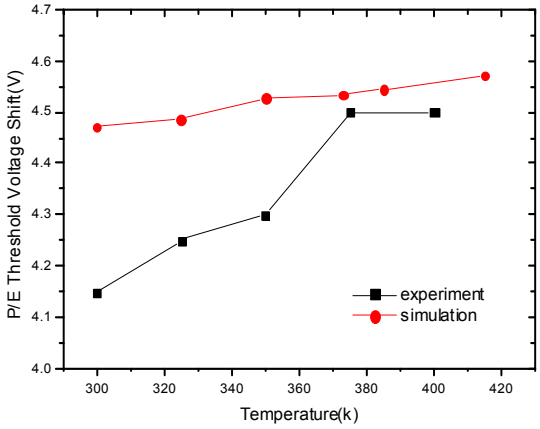
Where V_T is the threshold voltage, V_{FB} is the flat band voltage, Ψ_B is the physical parameter, $2\Psi_B$ is usually 0.6V, ε_S is the dielectric coefficient of silicon, q is the

electron charge value, N_A is the doping concentration of the p-type substrate, VBS is the base end bias substrate, C_o is the tunnel layer capacitance value.

When the temperature rises, the energy band of the flash memory is reduced, resulting in a change in the threshold voltage. Similar phenomena have been reported in "Threshold voltage variations with temperature in MOS transistors" [5] and other literature. Fig. 4(b) is a graph showing the threshold voltage shift between the writing and erasing operations of flash memory measured and simulated at different temperatures (300 to 415 ^{o}K). As can be seen from the figure, when the temperature is higher, the threshold voltage shift between the writing and erasing of the flash memory of the measurement and simulation is getting larger and larger, which means that the flash memory performs better at writing and erasing at high temperature than room temperature. However, because some models or parameters in the simulation do not take into account changes in temperature, thus the results of the simulation show no temperature effect.



(a)

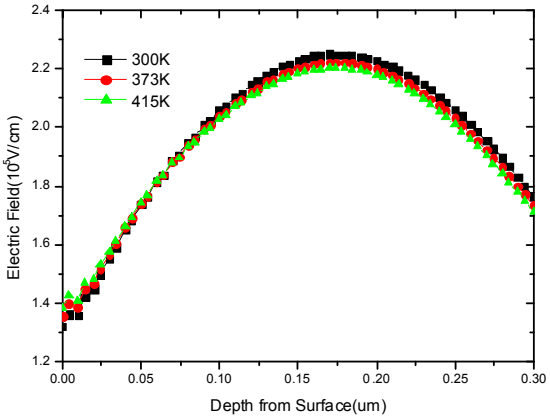


(b)

Figure 4 Graph of (a) threshold voltage, (b) threshold voltage shift for experimentally measured and simulated flash memory write and erase operations at different temperatures (300 to 415 ^{o}K).

Fig. 5 is a comparison of 1D electric field at a depth of (a)0.3um, (b)0.06um from the junction of oxide and substrate in a lateral position at 1.23um from the drain when the simulated flash memory is written at 300 ^{o}K, 373 ^{o}K and 415 ^{o}K. In Fig. 5(a), the vertical depth of 0.07um is set as a boundary, when the vertical depth is between 0~0.07um, the higher the temperature, the larger the electric field on the tunnel surface, and when the vertical depth is between 0.07~0.3um, the higher the temperature, the smaller the electric field at the surface of the tunnel. This is because at the vertical depth between 0~0.07um is a strong inversion layer of the tunnel where most electrons flow. Due to the temperature effect and the drain and gate bias, the temperature rises and the electrons of the substrate mostly flow to the surface of the tunnel, thus increasing the lateral potential of the tunnel surface, so that the higher the temperature, the larger the electric

field at the surface of the tunnel. Likewise, for the electric field value of the substrate, the higher the temperature the smaller the electric field value. However, because the electric field value at the surface of the tunnel is the key to affecting the maximum electron injection, the electric field curve with a vertical depth of 0~0.07um when viewed after being magnified, we can see from Fig. 5(b) that the electric field value of the tunnel surface at higher temperature is significantly higher than the electric field value at a lower temperature.



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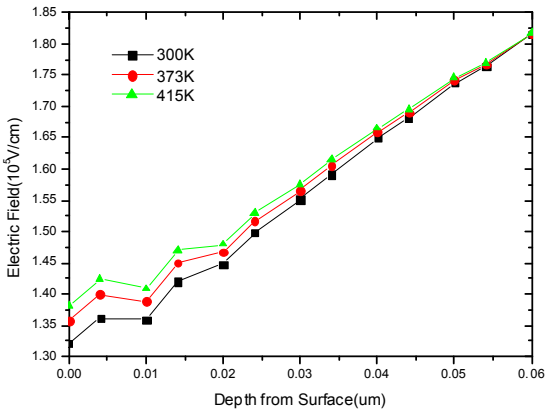


(b)

Figure 5 Comparison of 1D electric field from the junction of the oxide and substrate at a depth (a) 0.3um, (b) 0.06um in the lateral position at 1.23um near the drain during write operations of the simulated flash memory at 300 ^{o}K, 373 ^{o}K and 415 ^{o}K.

Fig. 6 is a comparison of 1D electric field at a depth from the junction of oxide and substrate in a lateral position at 1.23um from the drain when the simulated flash memory is written at 300 ^{o}K, 373 ^{o}K and 415 ^{o}K. As can be seen from the description of Fig. 5, the higher the temperature, the larger the electric field value of the tunnel surface, so that the higher the temperature, the greater the electron injection probability of the tunnel surface. As can be seen from this figure, when the vertical depth is greater than 0.05um, the probability of electron injection is close to zero. Because the incident electrons are concentrated on the tunnel surface, the factor that affects the maximum electron injection is the electric field value at the tunnel surface. Henceforth, as shown in Fig. 5(a), when the vertical depth is 0.07~0.3um, the lower the temperature, the larger the electric field value on the surface of the tunnel but when the depth is greater than 0.05um, there is no incident electron.

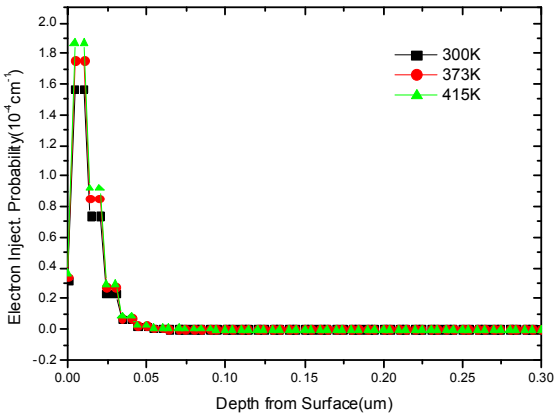
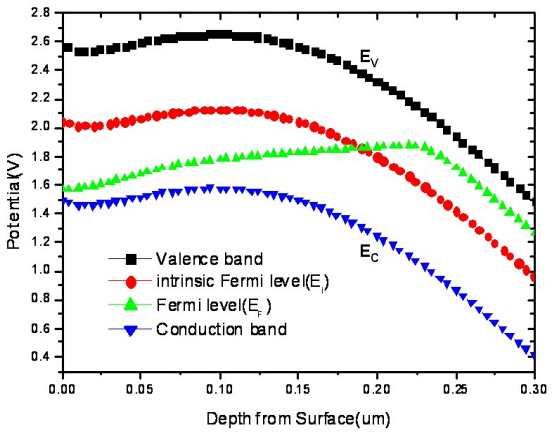
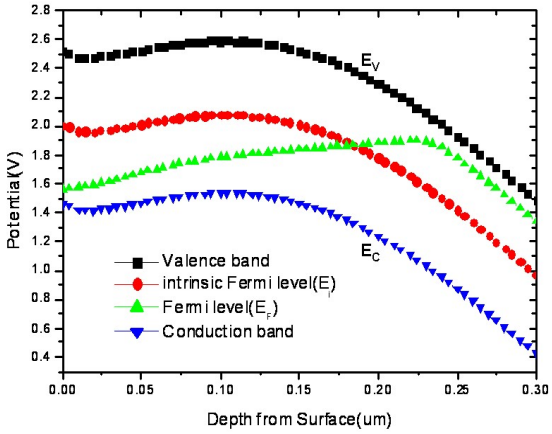


Figure 6 Comparison of electron injection probability rate at 1D depth from the junction of oxide and substrate in a lateral position at 1.23um near the drain during simulated flash memory write operations at 300 ^{o}K, 373 ^{o}K, and 415 ^{o}K.

Fig. 7 shows an 1D potential graph of the lateral position of 1.23um near the drain from the vertical depth of the junction of the oxide and substrate when the simulated flash memory is written at (a) 300 ^{o}K, (b) 373 ^{o}K, and (c) 415 ^{o}K. It can be seen from the three graphs that the inversion layer is generated on the surface of the substrate due to the relationship between the gate and the drain bias, which is known by the tunnel electron concentration equation $n= nie^{(E_F-E_i)/kT}$ (E_F: Fermi level, E_i: intrinsic Fermi level), the size of the tunnel electron flow depends on the value of E_F-E_i. Therefore, the higher the temperature, the smaller the value of E_F-E_i, which means that the higher the temperature, the more holes are added than the electrons, so the smaller the number of electrons, but the difference in the number of electrons is not large. However, since the flash memory has a large electric field and electron injection probability at a high temperature, the operation performance is preferably at a high temperature.



(a)



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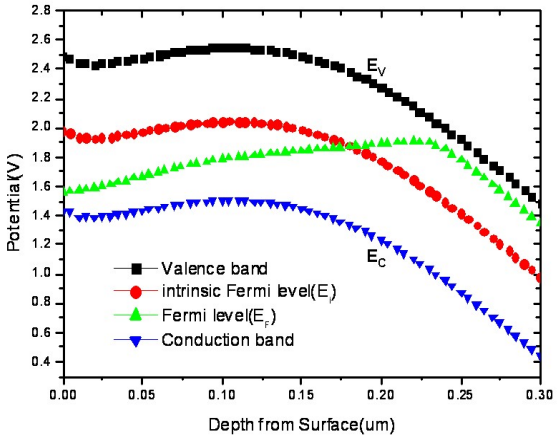

(c)

Figure 7 Potential graph at 1D depth from the junction of oxide and substrate in a lateral position at 1.23um near the drain during simulated flash memory write operations at 300 ^{o}K, 373 ^{o}K, and 415 ^{o}K.

IV、CONCLUSIONS

From the above analysis and comparison, it can be seen from the writing and erasing characteristics of the flash memory measurement and simulation that as the ambient temperature rises, the writing and erasing performance of the flash memory at high temperature is higher than that at room temperature. The write and erase threshold voltages of the flash memory are slightly decreased as the operating temperature rises, and have a variation of -4 mV/^{o}c to -2 mV/^{o}c. When the temperature is higher, the threshold voltage shift between the measurement and simulation flash memory writing and erasing operations is getting larger and larger. In addition, the surface electric field and electron injection probability of the flash memory increase at high temperature with the increase of temperature, but when the simulated flash memory is written, in the lateral position at 1.23um near the drain, and this can be seen from characteristic curve of the potential graph at 1D vertical depth from the junction of oxide and substrate. The higher the temperature, the smaller is the electron concentration of the tunnel, but the difference is not large, so the overall operation performance is still better at high temperature.

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高溫下快閃記憶體元件操作效能之研究

何家淮[1*] 羅慶同[2] 熊漢琳[3]

[1]康寧大學視光科
[2]陸軍專科學校電腦與通訊工程科
[3]康寧大學企管系
*Corresponding author: Tel:886-933-532016; E-mail address: jh.ho@msa.hinet.net

摘要

近年來隨著半導體製程技術之進步，使得積體電路之尺寸愈做愈小而功能性則愈來愈高，但伴隨著元件之微小化，因封裝技術之限制及元件積集度之增大，將使得元件所在工作環境之溫度上升，所以溫度變化對快閃記憶體效能之影響就顯得非常的重要，本論文即是針對快閃記憶體於高溫環境下之操作效能來進行研究與探討。

在本論文中，首先透過 flash 元件實驗量測之操作效能值與模擬之效能值進行比較，得到一致之性能趨勢後，再用模擬之數據來分析與說明 flash 元件於室溫及高溫環境下，其效能表現之差異。

實驗分析顯示，flash 元件之臨界電壓是隨操作環境溫度之上升而略為下降的，當溫度愈高時，量測及模擬之 flash 元件寫入及抹除操作之臨界電壓差均愈來愈大。且 flash 元件在高溫時之通道表面電場值及電子注入機率均較大，然因溫度效應使得高溫時之通道電子濃度較小，惟與室溫時相較差別並不大，所以操作效能仍以高溫時為佳。

關鍵詞：快閃記憶體、操作效能、 MEDICI、臨界電壓差、能帶圖